Specification Amendments

Please replace the paragraph beginning on page 1, line 14 with the following text:

This application is a continuation of United States application Serial No. 09/513,538, filed 25 February 2000, now U.S. Patent No. ~~_,___,___~~ 6,643,317.

Please replace the paragraph beginning on page 8, line 3 with the following text:

By driving flip-flop 54 at half the frequency, NMOS switch 60 is caused to alternate every other clock period between non-delayed clock signal 32 and the delayed clock signal at a rate parsing one pulse into two spectral components. Concurrently, the parsed pulses may then be reaggregated to create a digitally spread output clock signal pulse, resulting in a spread spectrum signal 80. The period of each digitally spread clock signal pulse is alternatively longer or shorter than that of the original [[dock]] clock pulse. The length of the spread pulse is determined by delay time D of the RC timing circuit 30. The length of signal delay D is controlled by the operating characteristics of the selected resistor circuit 30 and the capacitance of capacitor 70.

Please replace the paragraph beginning on page 8, line 12 with the following text:

Again, by driving flip-flop 54, and hence, NMOS switch 60 at half the clock frequency of primary clock signal 22 frequency, spread spectrum system 10 generates a spread spectrum output pulse signal 80 composed of portions of the original clock pulse and portions of the original clock pulse delayed by the amount of delay time D inherent within RC timing circuit 30 and 70. The period T of the pulse is expanded or contracted by the amount of delay time D inherent within [[AC]] RC timing circuit 30, while the total energy of the pulse remains substantially constant. Consequently, having spread the energy of a single clock pulse over a period of T + D and T - D, while the total pulse energy remains constant, the amplitude of the outputted spread spectrum pulse is lower at both the nominal frequency and harmonics of that frequency. Hence, by varying the delay time D of RC timing circuit 30 and 70, the spread in frequency of signal 80 can be adjusted with infinite granularity. The generated spread spectrum clock signal 80

provides desired system synchronization via generation of a specific nominal frequency while minimizing radiation of undesirable EMI.

Please replace the paragraph beginning on page 9, line 3 with the following text:

A state machine 150 receives an input from original primary clock signal 122 which synchronizes operation of state machine 150 with operation of multiplexer 140. In this second embodiment 110, state machine 150 generates three states 111 (FIG. 2b) sequentially inputted to multiplexer 140 via a line 152. FIG. 2b is a block diagram of the state machine from FIG. 2a selecting the different inputs to the multiplexer.

Please replace the paragraph beginning on page 9, line 9 with the following text:

Referring now to both FIGS. 2a and 3, the timing diagram provided in FIG. 3 illustrates the discrete operation of single delay line embodiment 110 of the spread spectrum system according to the invention. The timing diagram shows the original non-delayed clock signal 122 and delayed clock signal 131 as each having equal periods of 1. Delay line 130 has an inherent delay time of D/Ll. When flip-flop [[140]] 141 of the 2-bit state machine 150 is low, it issues a low signal 152 on the SEL pin which causes multiplexer 140 to select and output non-delayed signal 122 present at the primary clock signal input pin CLK 142. When flip-flop [[140]] 141 of the 2 bit state machine 150 is high, it issues a high signal 152 on the SEL pin which causes multiplexer 140 to select and output delayed signal 131 present at delay line input pin A 144.

Please replace the paragraph beginning on page 9, line 20 with the following text:

State machine 150 and multiplexer 140 cooperate to parse, sample, and reaggregate original clock signal 122 and delayed signal 131 to provide an output spread spectrum clock signal 180 whose period switches alternatively between T, [[T+DL1]] T+D/L1, [[T-DL1]] T-D/L1 decreasing the peak energy at the main frequency of f = 1/T

of the primary clock signal. The total energy is effectively spread to three frequencies at f1 = 1/T, ~~f2 = 1/(T+DL1)~~ f2 = 1/(T+D/L1) and ~~f3 = 1/(T-DL1)~~ f3 = 1/(T-D/L1). Thus, depending on input original clock signal 122, the delay time D/Ll inherent in delay line 130, the selection of multiplexer 140 input by the state machine 150, one is able to design a spread spectrum system circuit configuration according to the invention that is capable of generating a plurality of different aggregate output spread spectrum clock signals 180.

Please replace the paragraph beginning on page 10, line 9 with the following text:

This dual delay line embodiment 210 of the spread spectrum system is thus capable of generating three signals: the original non-delayed clock signal 222, the D1 clock signal 231, and the D3 clock signal 233. Each clock signal 222, 231, 233 is routed to separate input pins 242, 244, 246 of a 3 to 1 multiplexer 240, which is then able to sample each of signals 222, 231, 233. Accordingly, viewing the discrete operation of the dual delay line spread spectrum, original non-delayed clock signal 222 is parsed, sampled, and reaggregated to provide output spread spectrum signal 280 having a period of T+D1+D2 or T+3*D1. Consequently, the period of outputted spread spectrum signal [[180]] 280 is lengthened or reduced while the total energy of the signal remains constant. Accordingly, the amplitude of the signal at all frequencies is substantially lowered, thereby reducing the level of EMI produced at the nominal frequency and all harmonics thereof during the generation of the signal. The timing diagram associated with the discrete operation of this preferred embodiment is provided in FIG. 5 to illustrate how the addition of one more delay line substantially increases the number of possible configurations for the resulting spread spectrum signal 280.